Wednesday, July 21

Session 6: Evolution of CA and Brain-Inspired Architectures I Chair: S. Colombano, NASA ARC, USA

9:00 - 9:30 P. Marchal, Centre Suisse d' Electronique et de Microelectronique SA, Switzerland
Embryological Electronics

9:30 - 9:55 H. de Garis, A. Buller, M. Korkin, F. Gers, N. Nawa, M. Hough, ATR, Japan; Technical University of Gdansk, Poland; Genobyte Inc., USA; IDSIA, Switzerland; Stanford University, USA
ATR's Artificial Brain (CAM-Brain) Project: A Sample of what Individual "CoDi-1 Bit" Model Evolved Neural Net modules can do with Digital and Analog I/C

9:55 - 10:20 V. Vassilev, J. Miller, T. Fogarty, Napier University, UK
Co-evolving Demes of Non-Uniform Cellular Automata for Synchronisation

10:20 - 10:45 C. Ortega, A. Tyrrell, University of York, UK
Reliability Analysis in Self-Repairing Embryonic Systems

10:45 - 11:00 *Break*

Session 7: Evolution of CA and Brain-Inspired Architectures II Chair: A. Thakoor, JPL, USA

11:00 - 11:20 M. Perkovski, Portland State University, USA; A. Chebotarev, Glushkov Institute of Cybernetics, Ukraine; A. Mishchenko, Portland State University, USA
Evolvable Hardware or Learning Hardware? Induction of State Machines from Temporal Logic Constraints

11:20 - 11:40 E. Mjolsness, E. Meyerowitz, V. Gor, T. Mann, Jet Propulsion Laboratory, USA
Morphogenesis in Plants: Modeling the Shoot Apical Meristem, and Possible Applications

11:40 - 12:00 P. Davis, ATR Adaptive Communications Research Laboratories, Japan
Adaptive Networks with Self-Organizing Multi-Hop Links

Session 8: Reconfiguration Architectures Chair: A. Hunsberger, NSA, USA

12:00 - 12:20 R. Porter, K. McCabe, Los Alamos National Laboratory, USA; N. Bergmann, Queensland University of Technology, Australia
An Application Approach to Evolvable Hardware

12:20 - 12:40 N. Macias, USA
The PIG Paradigm: The Design and Use of a Massively Parallel Fine Grained Self-Reconfigurable Infinitely Scalable Architecture

12:40 - 2:00 *Lunch*

Session 9: Advanced Reconfigurable Devices Chair: J. Moreno, Technical University of Catalunya, Spain

2:00 - 2:20 J. Moreno, J. Madrenas, J. Cabestany, E. Canto, Technical University of Catalunya, Spain; R. Kielbik, Technical University of Lodz, Poland; J. Faura, J.M. Insenser, SIDSA, PTM, Spain
Realization of Self-Repairing and Evolvable Hardware Structures by Means of Implicit Self-Configuration

2:20 - 2:40 J. McDonald, B. Goda, Rensselaer Polytechnic Institute, USA
Reconfigurable FPGA's in the 1-20 GHz Band with HBT BiCMOS

2:40 - 3:00 K. Asari, Y. Mitsuyama, T. Onoye, I. Shirakawa, H. Hirano, T. Honda, T. Otsuki, T. Baba, T. Meng, Matsushita Electronics Corp., Japan; Osaka University, Japan; Panasonic Technologies, USA; Stanford University, USA
FeRAM Circuit Technology for System on a Chip

3:00 - 3:10 *Break*

Session 10: GA Applications Chair: B. Toomarian, JPL, USA

3:10 - 3:30 T. Cwik, G. Klimeck, Jet Propulsion Laboratory, USA
Genetically Engineered Microelectronic Infrared Filters

3:30 - 3:50 G. Klimeck, C. Salazar-Lazaro, A. Stoica, T. Cwik, Jet Propulsion Laboratory, USA
Genetically Engineered Nanoelectronics

3:50 - 4:10 P. van Remortel, T. Lenaerts, B. Manderick, Brussels Free University, Belgium
The Evolution of ROBDDs: Preliminary Results and a First Analysis

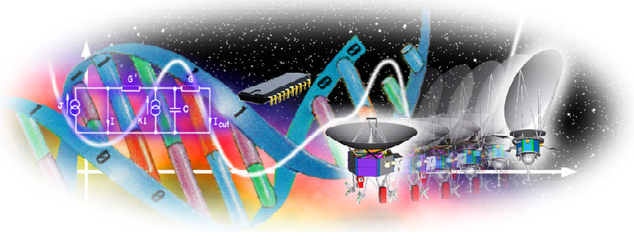
4:10 - 4:30 J. Masner, J. Cavalieri, J. Frenzel, J. Foster, University of Idaho, USA
Representation and Robustness for Evolved Sorting Networks

4:30 - 4:50 P. Chongstitvatana, C. Aporntewan, Chulalongkorn University, Thailand
Improving Correctness of Finite-State Machine Synthesis from Multiple Partial Input/Output Sequences

4:50 - 5:00 *Conclusions*

The First NASA/DoD Workshop on Evolvable Hardware

July 19 – 21, 1999
Jet Propulsion Laboratory
California Institute of Technology
Pasadena, California, USA



Sponsors
National Aeronautics and Space Administration (NASA)
Defense Advanced Research Projects Agency (DARPA)
Ballistic Missile Defense Organization (BMDO)

Hosts
Center for Integrated Space Microsystems (CISM), JPL
Center for Space Microelectronics Technology (CSMT), JPL
NASA Technology Program (NTP), JPL

Honorary Chair
John R. Koza, Stanford University

Chair
Adrian Stoica, Jet Propulsion Laboratory

Co-Chairs
Didier Keymeulen, Jet Propulsion Laboratory/ Electrotechnical Laboratory
Jason Lohn, NASA Ames Research Center

Program Committee
Leon Alkalai, Jet Propulsion Laboratory (USA)
Forrest H. Bennett III, Genetic Programming, Inc. (USA)
Gregory Cain, Victoria University (Australia)
Silvano P. Colombano, NASA Ames Research Center (USA)
Hugo de Garis, Advanced Telecommunication Research Lab (Japan)
Stuart J. Flockton, University of London (UK)
Terry Fogarty, Napier University (UK)
David B. Fogel, Natural Selection, Inc. (USA)
Inman Harvey, University of Sussex (UK)
Hitoshi Hemmi, NTT Communication Science Labs (Japan)
Tetsuya Higuchi, Electrotechnical Laboratory (Japan)
Lorenz Huelsbergen, Bell Labs, Lucent Technologies (USA)
Alan Hunsberger, National Security Agency (USA)
Rich Katz, NASA Goddard Space Flight Center (USA)
Benard Manderick, Vrije Universiteit Brussel (Belgium)
Daniel Mange, Swiss Federal Institute of Technology (Switzerland)
Pierre Marchal, Centre Suisse d'Electronique et de Microtechnique SA (Switzerland)
Julian Miller, Napier University (UK)
Eric Mjolsness, Jet Propulsion Laboratory (USA)
José Muñoz, Defense Advanced Research Projects Agency (USA)
Masahiro Murakawa, University of Tokyo (Japan)
Edward Rietman, Bell Labs, Lucent Technologies (USA)
Justinian Rosca, Siemens Corporate Research (USA)
Mehrdad Salami, Victoria University (Australia)
Eduardo Sanchez, Swiss Federal Institute of Technology (Switzerland)
Moshe Sipper, Swiss Federal Institute of Technology (Switzerland)
Stephen Smith, Altera (USA)
Stephen Trimberger, Xilinx (USA)
Adrian Thompson, University of Sussex (UK)
Anil Thakoor, Jet Propulsion Laboratory (USA)
Benny Toomarian, Jet Propulsion Laboratory (USA)
Ricardo Salem Zebulum, University of Sussex (UK)

The First NASA/DoD Workshop on Evolvable Hardware (EH'99) will be held at the Pasadena Convention Center, in Pasadena, California and hosted by the Jet Propulsion Laboratory. The purpose of this workshop is to bring together leading researchers from the evolvable hardware community, representatives of the programmable/reconfigurable hardware community, technology developers, and end-users from the aerospace community.

The emerging field of Evolvable Hardware is expected to have major impact on deployable systems for space missions and defense applications that need to survive and perform at optimal functionality during long duration in unknown, harsh and/or changing environments. Examples of such applications include outer solar system exploration, missions to comets and planets with severe environmental conditions, long lasting space-borne surveillance platforms, defensive counter-measures, long-term nuclear waste and other hazardous environment monitoring and control. Evolvable hardware is also expected to greatly enrich the area of commercial applications in which adaptive information processing is needed; such applications range from human-oriented hardware interfaces and internet adaptive hardware to automotive applications.

The purpose of the workshop is to provide a forum for discussion on the potential role of evolvable hardware in real-world applications, in particular those related to space. The Workshop attendees will have the opportunity to discuss the fundamental issues and state-of-the-art of evolvable hardware technology, plans for development of future devices and hardware systems suitable for evolution, and needs related to space applications. The outcome of this meeting is expected to be a technology development roadmap that would lead to deployable evolvable hardware.

Registration & check-in information

The meeting will begin at 8:50 A.M. on Monday, July, 19, at the Pasadena Convention Center in Room C107. This room is located on the first floor of the convention building, adjacent to the lobby. There is underground parking at $6.00/day; access is off of Euclid Street south of the convention building. On-site check-in will begin at 8:30 A.M. at the meeting site. At this time, you will be given your meeting badge and receipt for the registration fee, plus a packet of meeting materials. All participants will be expected to pay the workshop registration fee of $120.00 which covers the cost of the workshop, plus break service, a reception Monday, July 19 and a group dinner Tuesday, July 20. Please make checks payable to Caltech and forward per instructions on the registration form. Note that no credit cards, purchase orders, foreign checks or foreign currency can be accepted. For our planning purposes, pre-registration by July 1, with payment of fees is appreciated.

Accommodation and transportation

A block of rooms has been set aside at the Pasadena Holiday Inn at the current goverment rate of $95/single or double occupancy plus tax. The hotel will hold the room block until June 27, 1999 or until it is filled, after which time they will honor the rate on a space available basis only. You are responsible for making you own arrangements directly with the hotel. The Pasadena area is served by three major airport: LAX, Burbank and Ontario. Hourly airport bus service is available from LAX (all terminals) to the Holiday Inn from 8am until 9pm, with the transit time approximately one hour. To board the bus, exit the baggage claim area outside the terminal, look at the red bus sign located on the central island and wait for the bus labeled "AIRPORT BUS" with destination Pasadena. There are also several shuttles which provide door-to-door, on-call van service from the airports to Pasadena. Taxis and rental cars are also readily available at the airports and in Pasadena. For futher information, call the transportation services.

The Pasadena Holiday Inn
303 East Cordova
Pasadena, CA 91101
Ph: 626-449-4000 FAX: 626-796-6209
Reference: Evolvable Hardware

Transportation
Airport Bus: 714/938-8900 or 800/772-5299
Super Shuttle: 818/443-6600
Prime Time: 818/504-3600 or 800/262-7433

For further information please check the workshop web site or contact

Web Site: http://cism.jpl.nasa.gov/events/nasa_eh

Technical: Adrian Stoica
adrian.stoica@jpl.nasa.gov
Tel: +1 (818) 354-2190
Fax: +1 (818) 393-1545

Conference Logistics: Pat McLane
conf.admin@jpl.nasa.gov
Tel: +1 (818) 354-5556
Fax: +1 (818) 393-4992

Monday, July 19

8:50 - 9:00 — A. Stoica, Workshop Chair
J. Koza, Honorary Chair
Welcome and Organizational Remarks

9:00 - 9:15 — M. Chahine, JPL Chief Scientist, USA
Welcome Address

9:15 - 9:40 — W. Huntress Jr., Carnegie Institution of Washington, USA
NASA Rediscovers Technology

9:40 - 10:10 — L. Alkalai, Jet Propulsion Laboratory, USA
Micro/Nano Systems for Future NASA Grand Challenges in Deep Space Exploration

10:10 - 10:55 — J. Muñoz, DARPA, USA
DARPA's Adaptive Computing System Program

10:55 - 11:10 — *Break*

11:10 - 11:50 — I. Parmee, Plymouth University, UK
Identifying Requirements of Evolutionary Design Search, Exploration and Optimisation

11:50 - 12:30 — T. Higuchi, Electrotechnical Laboratory, Japan
Evolvable Hardware for Industrial Applications

12:30 - 1:45 — *Lunch*

Session 1: Evolution on FPGAs — Chair: J. Miller, Napier University, UK

1:45 - 2:10 — J. Miller, Napier University, UK
On the filtering properties of Evolved Gate Arrays

2:10 - 2:35 — D. Levi, S. Guccione, Xilinx Inc., USA
Genetic FPGA: Evolving Stable Circuits on Mainstream FPGA Devices

2:35 - 3:00 — G. Tufte, P. Haddow, The Norwegian University of Science and Technology, Norway
Prototyping a GA Pipeline for Complete Hardware Evolution

3:00 - 3:25 — E. Damiani, A. Tettamanzi, Universita degli Studi di Milano, Italy; V. Liberali, Universita degli Studi di Pavia, Italy
On line Evolution of FPGA-based Circuits: A Case Study on Hash Functions

3:25 - 3:40 — *Break*

Session 2: Design and Adaptation of Space Subsystems — Chair: R. Haupt, University of Nevada, USA

3:40 - 4:05 — W. Crossley, Purdue University, USA
Optimization for Aerospace Conceptual Design through the use of Genetic Algorithms

4:05 - 4:30 — J. Pollack, H. Lipson, P. Funes, S. Ficici, G. Hornby, Brandeis University, USA
Coevolutionary Robotics

4:30 - 4:55 — R. Haupt, J. Johnson, University of Nevada, Reno, USA
Dynamic Phase-Only Array Beam Control Using a Genetic Algorithm

4:55 - 5:20 — D. Linden, Linden Innovation Research LLC, USA; E. Altshuler, Air Force Research Laboratory, USA
Evolving Wire Antennas using Genetic Algorithms: A Review

5:20 - 5:45 — M. Buehler, Jet Propulsion Laboratory, USA
The Effects of Extreme Environments on Measurement Equipment

5:45 - 6:10 — A. Avizienis, University of California, Los Angeles, USA
The Hundred Year Spacecraft

7:00 - 8:30 — *Reception*
Athenaeum, California Institute of Technology

Tuesday, July 20

9:00 - 9:45 — J. Koza, Stanford University, USA
Evolving Circuits by Means of Natural Selection

Session 3: Evolution of Analog and Mixed-Signal Circuits — Chair: F. Bennett III, Genetic Programming Inc, USA

9:45 - 10:10 — R. Zebulum, M. Pacheco, M. Vellasco, University of Sussex, UK; Centro de Inteligencia Computacional Aplicada, Brasil
Artificial Evolution of Active Filters: A Case Study

10:10 -10:35 — A. Stoica, D. Keymeulen, R. Tawel, C. Salazar-Lazaro, W. Li, Jet Propulsion Laboratory, USA
Evolutionary Experiments with a Fine-Grained Reconfigurable Architecture for Analog and Digital CMOS Circuits

10:35 - 10:50 — *Break*

10:50 - 11:20 — A. Thompson, University of Sussex, UK
Explorations in Design Space: Can Evolutionary Algorithms Practically Search beyond the Scope of Conventional Electronics Design?

11:20 - 11:45 — P. Layzell, University of Sussex, UK
Inherent Qualities of Circuits Designed by Artificial Evolution: A Preliminary Study of Populational Fault Tolerance

11:45 - 12:10 — J. Lohn, G. Haith, S. Colombano, D. Stassinopoulos, NASA Ames Research Center, USA
A Comparison of Dynamic Fitness Schedules in Automated Amplifier Design

12:10 - 12:35 — S. Flockton, K. Sheehan, University of London, UK
A System for Intrinsic Evolution of Linear and Non-linear Filters

12:35 - 2:00 — *Lunch*

Session 4: Evolution of Digital Functions — Chair: A. Thompson, University of Sussex, UK

2:00 - 2:25 — V. Vassilev, J. Miller, T. Fogarty, Napier University, UK
On the Nature of Two-Bit Multiplier Landscapes

2:25 - 2:50 — A. Hernandez-Aguirre, Tulane University, USA; C. Coello, Laboratorio Nacional de Informatica Avanzada, Mexico; B. Buckles, Tulane University, USA
A Genetic Programming Approach to Logic Function Synthesis by Means of Multiplexers

2:50 - 3:15 — T. Kalganova, J. Miller, Napier University, UK
Evolving More Efficient Digital Circuits by Allowing Circuit Layout Evolution and Multi-objective Fitness

3:15 - 3:30 — *Break*

Session 5: Dynamic Reconfiguration — Chair: S. Casselman, Virtual Computer, Corp., USA

3:30 - 3:55 — G. Lu, H. Singh, M. Lee, N. Bagherzadeh, F. Kurdahi, University of California at Irvine, USA; E. Filho, V. Alves, COPPE/Federal University of Rio de Janeiro, Brazil
The MorphoSys Dynamically Reconfigurable System-On-Chip

3:55 - 4:20 — G. Milne, University of South Australia, Australia
A Model for Dynamic Adaptation in Reconfigurable Hardware System

4:20 - 4:30 — *Break*

4:30 - 6:00 — Panel: *The Future of Reconfigurable Computing Technologies*
Organizer and Moderator: J. Schewel, Virtual Computer Corp.
L. Alkalai, Jet Propulsion Laboratory; P. Athanas, Virginia Tech; S. Casselman, Virtual Computer, Corp.; D. Levi, Xilinx Inc.; S. Trimberger, Xilinx Inc.

7:00 - 9:00 — *Banquet*
Speaker: D. Fogel, Natural Selection, Inc., USA
Dusting off Some Old Evolvable Hardware